

CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

- 1 1. A method of improving the performance of
2 different semiconductor conductivities on the same
3 wafer comprising steps of
4 fabricating thin spacers on a wafer adjacent a
5 gate structure,
6 depositing a hard mask film across said wafer,
7 forming a block mask over a first transistor,
8 removing said hard mask film from a second
9 transistor,
10 forming a raised source-drain region by
11 selective epitaxy,
12 removing said block mask over said first
13 transistor,
14 performing additional selective epitaxial
15 growth, effecting only the areas of said second
16 transistor as said hard mask film covering said
17 first transistor is resistant to said additional
18 epitaxial procedure, and
19 performing extension implants to RSD regions of
20 at least one of said first or second transistor.
- 1 2. A method as recited in claim 1 in which said
2 performance improvements include at least one of
3 reducing series resistance,
4 subjecting extensions to low thermal budget
5 processing only,
6 providing independent offset for said first and
7 second transistors.

1 3. A method as recited in claim 1 wherein
2 said first transistor is an nFET, and
3 said second transistor is a pFET.

1 4. A method as recited in claim 3 wherein said
2 wafer is an SOI wafer.

1 5. A method as recited in claim 1 wherein said thin
2 spacers are comprised of
3 an SiN film followed by a SiN spacer etch,
4 wherein a thin SiO₂ liner may be deposited
5 prior to said SiN film and said SiN spacer etch with
6 the resulting thickness of the spacer ranging from
7 3-15 nm.

1 6. A method as recited in claim 5 comprising the
2 further steps of
3 removing the hard mask from said first
4 transistor,
5 defining a block mask protecting said second
6 transistor,
7 implanting extensions to said first transistor,
8 removing the block mask from said second
9 transistor,
10 defining a block mask protecting said first
11 transistor, and
12 implanting extensions to said second
13 transistor.

1 7. A method as recited in claim 6 further
2 comprising the step of fabricating source-drain
3 spacers.

1 8. A method as recited in claim 7 further
2 comprising the steps of
3 applying a first block mask over said second
4 transistor,
5 performing source-drain implants to said first
6 transistor,
7 removing said first block mask from said second
8 transistor,
9 applying a second block mask over said first
10 transistor,
11 performing source-drain implants to said second
12 transistor, and
13 removing said second block mask from said first
14 transistor.

1 9. A semiconductor apparatus comprising
2 a MOSFET device including Si wafer thinning,
3 isolation, gate dielectric, and gate stack
4 patterning,
5 a first transistor,
6 a second transistor,
7 thin sidewall spacers,
8 a thin epitaxial Si layer adjacent said thin
9 sidewall spacers of a first transistor, and
10 a thick epitaxial Si layer in the extension
11 region of a second transistor.

1 10. An apparatus as recited in claim 9 wherein said
2 MOSFET device is an ultra-thin Si channel MOSFET.

1 11. An apparatus as recited in claim 9 further
2 comprising a block film stack over the first
3 transistor.

1 12. An apparatus as recited in claim 9 further
2 comprising halo and extension implants in the region
3 of the first transistor.

1 13. An apparatus as recited in claim 12 further
2 comprising halo and extension implants in the region
3 of the second transistor.

1 14. An apparatus as recited in claim 13 further
2 comprising a source-drain spacers for said first and
3 second transistors.

1 15. An apparatus as recited in claim 14 further
2 comprising source-drain implants in regions of both
3 first and second transistors.